

The VFAT Production Test Platform for the TOTEM Experiment

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Abstract

VFAT is the front-end ASIC designed for the charge readout of silicon and gas detectors within the TOTEM experiment of the LHC. A stand alone portable Totem Test Platform (TTP) with USB interface has been developed for the systematic testing of the TOTEM hybrids equipped with VFAT chips. This paper is divided into 3 sections; the first describes the hardware features of the TTP, the second describes the software routines for the control and systematic testing of VFATs, the third presents the analysis and a sample of results.

I. INTRODUCTION

The front-end ASIC designed for the readout of silicon and gas sensors within the TOTEM [1] experiment at the LHC at CERN is called VFAT [2,3]. Two types of VFAT hybrid have been developed for the TOTEM silicon and gas sensors. Figure 1 shows a close-up view of 4 VFAT chips bonded to an edgeless silicon sensor intended for use within the TOTEM Roman Pots.

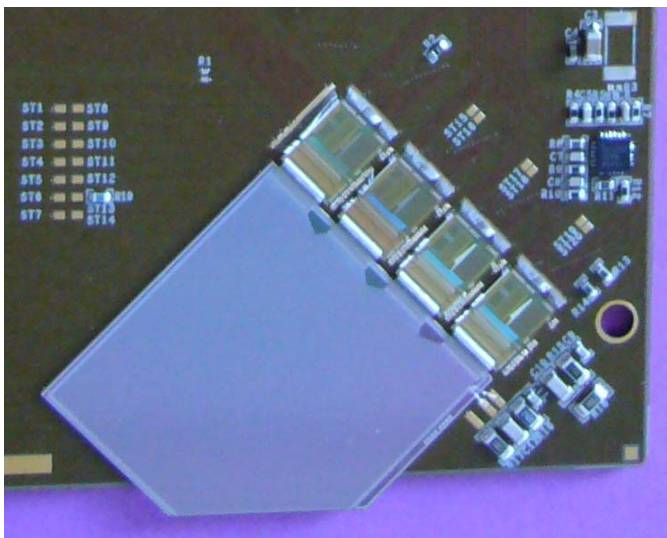


Figure 1 : A Roman Pot hybrid containing 4 VFAT chips bonded to an edgeless silicon sensor.

Figure 2 shows a VFAT hybrid designed for use with TOTEM GEM and CSC gas sensors.



Figure 2: VFAT mounted on a gas sensor hybrid. The chip and bond wires are protected from damage by a protective cap (not shown).

The Totem Test Platform (TTP) was conceived to be a “light” DAQ system for the production test of VFAT together with the hybrid. The goal was to have a compact and portable test bench for VFAT hybrids that can be controlled by USB connection from a laptop. Data is also read through the USB and data analysis software used to interpret the results. Further extensions to the use of the TTP as a “light” DAQ are also possible.

II. VFAT BRIEF OVERVIEW

VFAT [2,3] produces both “Trigger” and “Tracking” information. “Trigger” information, in the form of a programmable fast “OR”, can be used for trigger building. The “Tracking” information is in the form of binary “hit” channel data corresponding to a given clock period selected by a first level trigger (LV1A).

VFAT has 128 channel inputs. Each channel contains a low noise pre-amplifier and shaper followed by a comparator. Following the comparator are digital circuits used for generating the “Fast-OR” outputs, data storage and data packet construction.

On receipt of a trigger, the corresponding binary data is packaged together with time stamps into a data packet. The data packet has the form shown in Figure 3. Hence, for every trigger, the DAQ receives a data packet containing the individual VFAT identification no. (ChipID), the Bunch crossing no. (BC), trigger Event no. (EC) and the corresponding binary channel data. Also contained within the packet are, some status flags and a CRC check.

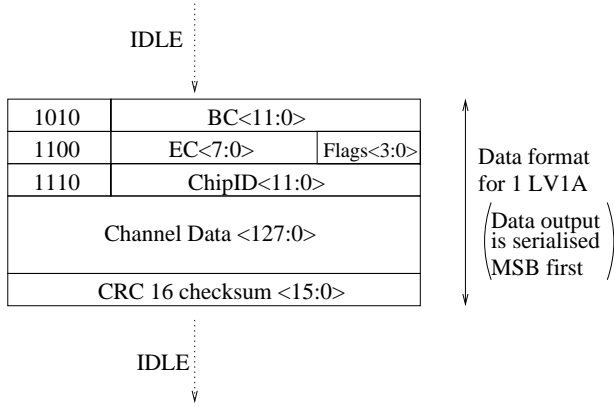


Figure 3 : The VFAT data packet corresponding to a triggered event.

VFAT has a multitude of programmable options which range from programmable biasing to testability options. A full list of programmable options is contained within [3]. One extremely useful feature is an internal programmable test pulse generator which can deliver a charge pulse to a given channel for test and calibration purposes. Variables include channel selection, the polarity of the charge, the amount of charge and the phase of the charge delivery within one clock period. The amount of charge is controlled by an internal DAC called “VCal”. Another important variable is the comparator threshold. The coarse comparator threshold is given by the difference of two DAC values called VT1 and VT2. Positive thresholds are obtained by fixing VT2=0 and varying VT1, Negative threshold by fixing VT1=0 and varying VT2. Individual “fine” threshold adjustments are also possible using 5 bit “TrimDACs” in each channel.

III. THE TTP HARDWARE DESIGN & ARCHITECTURE

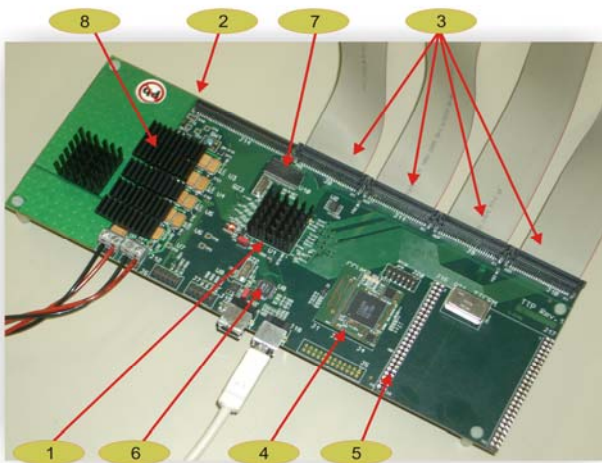


Figure 4: The TTP, itemizing its main components.

1. An FPGA (EP2C20F484C6N of the Cyclone II FPGA [4] family by Altera Corporation).
2. A Roman Pot hybrid socket.
3. Four GEM hybrid sockets.
4. An i²c master hybrid socket (CCUM, that hosts a custom rad-hard i²c master ASIC namely CCU25 [5]).
5. A clocking & triggering hybrid socket (TTCrm, that hosts a custom rad-hard ASIC namely TTCrx [6]).
6. A USB 2.0 full speed interface (FT245BL [7] by FTDI Ltd).
7. A USB 2.0 high-speed interface (CY7C68001-56PVC or “SX2” [8] by Cypress semiconductors).
8. Linear Regulators.

The TTP is a compact (26cm x 10 cm) card, a photograph of which is shown in Figure 4 and followed by an itemized list of its main components.

A block diagram for the TTP architecture is shown in Figure 5.

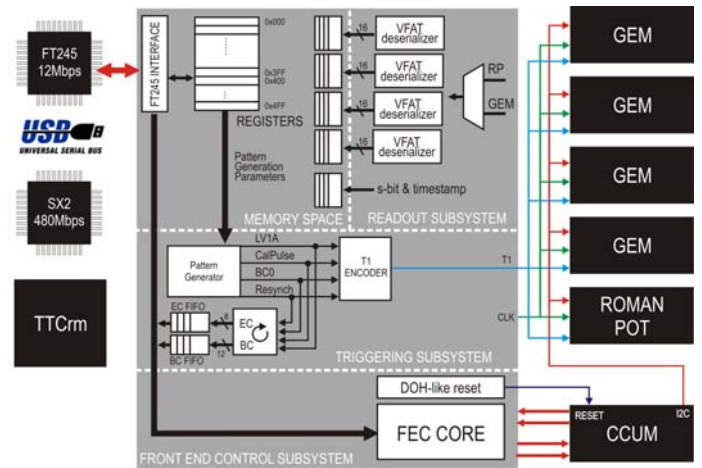


Figure 5: Block diagram of the TTP architecture.

The TTP architecture is largely based on an existing test bench developed for the CMS Preshower [9]. It can be divided into four main subsystems controlling the functions of Triggering, Readout, Front-end control and Local control.

A. The Triggering Subsystem

The purpose of the triggering subsystem is to provide timing and fast command information to the front-end chips in a programmable way in order to facilitate system tests. The four encoded fast T1 commands are generated as described in Table 1. The encoding scheme used is a 3-bit pattern, thus requiring 3 clock cycles to be transmitted through a single line. The first bit of the pattern is always ‘1’ denoting the existence of a fast command and the remainder which is being transmitted (“00”=LV1A, “01”=BC0, “10”=Resynch, “11”=CalPulse).

The triggering subsystem is developed in such way that it can generate bursts of triggers by specifying the time intervals between consecutive triggers expressed in no. of clock cycles.

Name	Description	Priority	Encoding
Resynch	Synchronising reset of the front-end chips	1 (highest)	110
BC0	Bunch crossing zero	2	101
CalPulse	Signal sent to the front-end to generate internal injection pulses	3	111
LV1A	Level 1 Trigger Accept	4 (lowest)	100

Table 1: The four fast T1 commands that can be sent by the triggering subsystem.

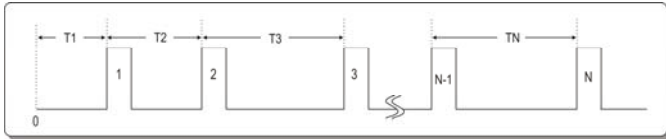


Figure 6 : Timing variables for the generation of multiple triggers by the pattern generator.

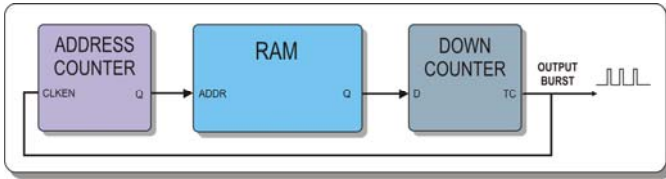


Figure 7: RAM based pattern generator implementation.

Figure 6 shows how a burst of pulses (each of one clock cycle width) can be defined by a sequence of numbers ($t_1, t_2, t_3 \dots t_N$). The implementation of the pattern generator is based on a RAM, where the values T_1, T_2, T_3 etc. are stored (Figure 7). Initially, the address counter is reset and therefore the first value (T_1) stored in RAM appears at its output. This value is loaded to the down counter. When the down counter reaches zero, the output initiates a pulse. At the same time the address pointer of the RAM is incremented providing the next value (T_2) to the decrementing counter and so on.

The triggering subsystem is able to generate bursts of up to 1024 LV1A (and/or CalPulses), with the time between two consecutive pulses being between 3 and 2^{32} clock cycles. The trigger bursts may appear in different ways depending on the internal triggering mode settings and other related parameters. Another feature of the system is that for every event, the corresponding event and bunch numbers are stored locally in two 256 word-deep FIFOs. By comparing the numbers stored in the FIFOs with the ones generated by VFAT included in every data packet, the user of the test bench can verify the synchronization with the front end system. The system can also accept trigger and clock signals provided from external sources. In addition, the ability to host a TTCrm module gives the possibility to interface with a standard TTC system.

B. Readout Subsystem

The readout subsystem consists of VFAT deserializers and FIFOs. The deserializers extract the 192-bit data packets from the 40Mbps serial data stream and format them in 16-bit words. The formatted packets are stored in 1024x16bit FIFOs, and therefore the maximum packet capacity per channel is 85.

C. Front-end control subsystem

For software backward compatibility, the test bench includes the functionality of the CMS Tracker FEC system for controlling front-end chips over an i²c bus. For this reason, the CCUM hybrid is used. The core of communication protocol with the CCU ASIC, known as FEC (front end control) has been included in the FPGA.

D. Memory Space

The memory space of the TTP includes a 1024x32bit RAM that stores trigger patterns as well as several registers used for setting the working parameters and providing status information of the test bench. The access of this memory space (as well as the direct FEC-core access) is done through the FT245 USB 2.0 full speed device hosted on the board. The FT245 communicates with the FPGA through an 8-bit bus. The FT245 interface implemented in the FPGA reads the byte-stream and decodes it according to the custom command protocol developed. The command protocol supports both single and burst read/write transactions.

IV. TTP SOFTWARE

There are 2 principal packages used by the TTP. The first is the “VFAT Controller” and the second is the Analysis Software. Both of these packages are needed to run the VFAT Test Procedures used to characterise VFATs. This section describes the VFAT Controller, Analysis Software and the Test Procedures.

A. The VFAT Controller

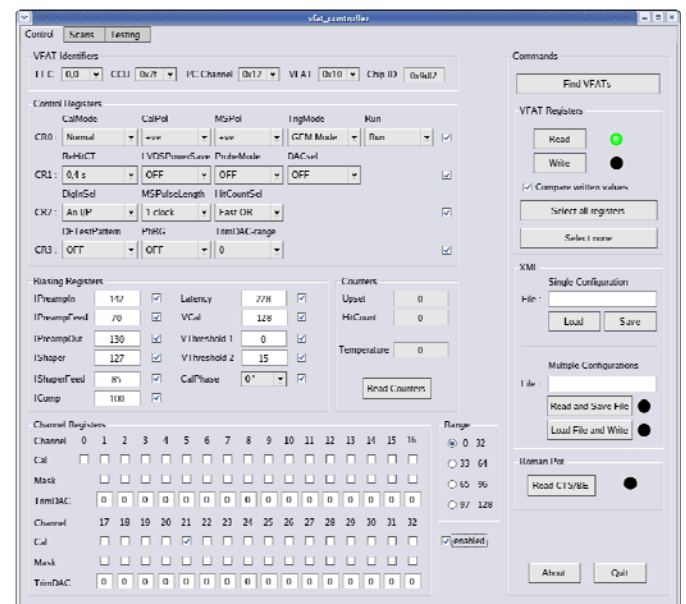


Figure 8: VFAT Controller first panel.

The VFAT controller is used (as it's name suggests) to control VFAT operation. The software was developed as a part of the FEC software package [10],[11] and the graphical user interface is based on the Qt libraries [12].

The first user panel is shown in Figure 8. This panel serves two functions. The first is a search for all components responding to I²C commands on the I²C bus. The results of the search are displayed on the top line indicating the number of VFATs found, their chip ID and other components such as CCU. The rest of the panel is used for downloading constants to the VFAT internal registers. In this way the VFAT mode of operation can be chosen and the biasing set-up. The panel also reads back from VFATs the downloaded parameters to verify the communication. A second VFAT Controller panel is used to command VFAT during manual tests and a third panel is used to select test procedures used in systematic chip testing. The different test routines available are described in part C of this section.

B. Analysis Software

The analysis software has been developed within the framework of the TOTEM Online Monitor [13]. It has two distinct parts; a graphical user interface based on Qt, and a data processing framework based on ROOT [14]. As a consequence it can be run in both interactive and batch modes.

The monitor takes three files as the input: a hardware configuration file, a binary data file and a VFAT I²C configuration file.

The hardware setup can be described as a tree. For example, one Roman Pot contains 10 hybrids, each hybrid has 4 VFATs and each VFAT has 128 channels. Each element in the tree is assigned a C++ class that can process event data and produce output plots or fit results.

The "Canvas layout" dialog shows the tree of all hardware elements in the left column. The right column shows the list of available output plots for the selected hardware element. This mechanism ensures that at each level of the tree, just the dedicated analysis is performed and the relevant plots are produced. Events are successively read from the binary data file (performing various consistency checks) and recursively processed through the element tree. Fits and production tests are performed and summary protocols are saved.

C. Test Procedures

The functions of the different routines available in the VFAT Controller are detailed in Table 2.

The results are then summarised in a summary file as well as fits and acceptance cuts. These summary files are stored in unique directories created from VFAT IDs and measurement timestamps. For detailed study; the results can be visualised by the analysis software.

Figure 9 shows plots of the response of DACs following the DAC scan. From these curves a precise knowledge of the analog biases and calibration of charge delivery can be obtained.

Name	Description
Power measurement	The power consumption is measured automatically for VFATs in "Sleep" and "Run" modes.
I ² C Check	Writes and reads to all VFAT internal registers and verifies the success of the operation.
Data packet check	Vigorously applies multiple triggers to VFAT and checks consistency of the data packets with a reference file. This routine checks the memory logic functions ie. counters, flags, CRC etc.
Mask check	Each channel is masked and then pulsed to verify "mask" functionality.
DAC scan	Routes the analog output of each DAC in turn to the DCU and scans the 8 bit DAC range. This is an important operation for calibration of the chip.
Pulse Scan	Characterisation of the analog performance such as noise and threshold. A channel is selected and an input charge swept through a fixed threshold providing data for S-curve analysis. Options include polarity of signal charge and High or Low resolution. High Res. instructs VFAT to inject charge to one channel at a time while Low Res. performs the procedure on many channels simultaneously.
Binary Scan	The binary scan is a quick method for identifying excessively noisy (singing) channels or dead channels. For each channel in turn, a constant signal charge is delivered a number of times well above threshold. A channel operating correctly will show the number of hits equal to the number of signal charge pulses (100%). A singing channel will also record hits when no signal charge is applied and hence will record greater than 100% whilst a dead channel 0%.

Table 2: Test routine options within the VFAT Controller

The results of the Pulse Scan can be viewed in the form of S-Curves. An S-Curve (shown in the top right hand plot of Figure 10) is a histogram of hits on a selected channel as a function of input pulse amplitude. Starting below threshold with 0% of hits and continuing to well beyond threshold (to 100% of hits) an "S" is formed. An error function fit to the curve yields the noise and threshold as the sigma and mean of the fit.

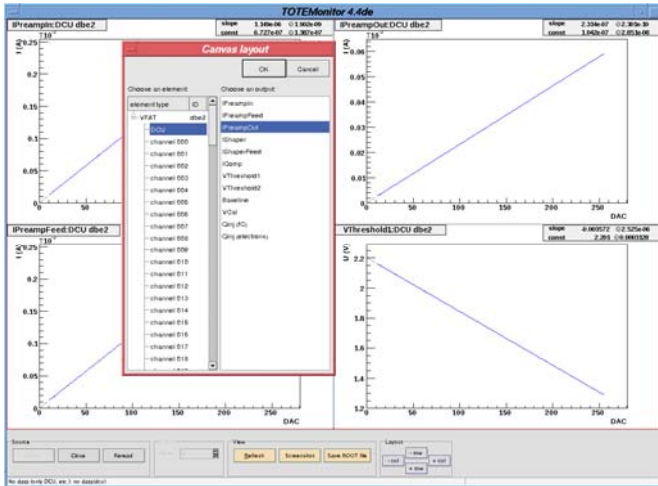


Figure 9: Plots of the response of internal VFAT DACs.

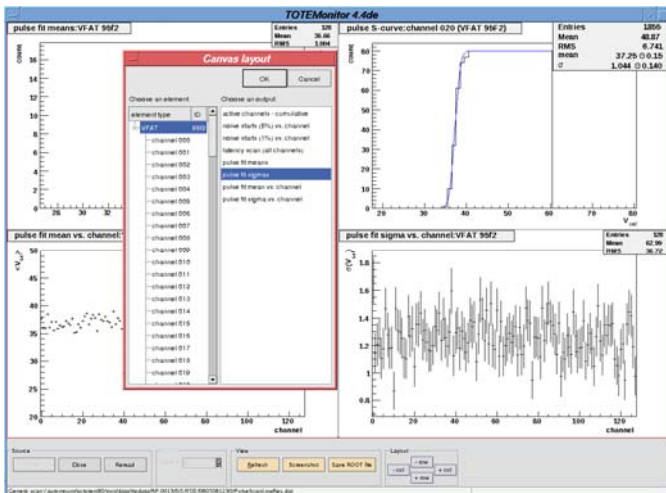


Figure 10: Analysis showing selection of an individual channel's S-curve (top right) and the noise as a function of channel number (bottom right)

Outputs from the binary scans are shown in Figure 11.

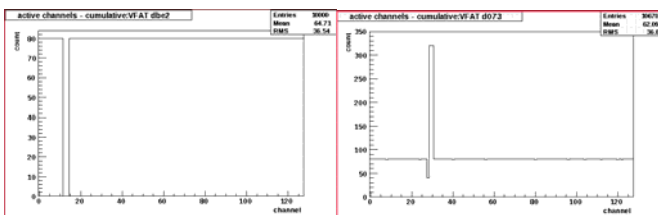


Figure 11: Results from a binary scan. Each of the 128 channels was pulsed 80 times in turn. A healthy channel returns 80 hits. The left hand plot identifies a dead channel (with 0 hits) and the right hand plot identifies a "singing" channel.

V. CONCLUSION

The stand alone portable test bench TTP (TOTEM Test Platform) has been described in this paper. It was developed for the production test of the TOTEM detector hybrids. It is also however, a more generally applicable portable data acquisition system for these detector hybrids with hardware, firmware and software in place. The silicon detectors are directly mounted on the Roman Pot hybrid, but the gas

detector hybrids are connected to the detector using the on-board connector. This makes it possible to test other detectors with a full readout chain from the flexible VFAT front end to the USB connection of a PC. Often the lack of such system is a bottleneck in detector development.

The FPGA and additional connectivity on the TTP also allows larger systems with one TTP operating as a master for several others, and evolution of the system to match the needs.

VI. REFERENCES

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